

CLAIMS

1. An apparatus comprising:

a first circuit configured to generate a plurality of difference values by calculating an absolute difference between each pixel from a current block and a corresponding pixel from a reference block substantially simultaneously;

a second circuit configured to generate a plurality of sum values by adding said difference values; and

a third circuit configured to generate at least one motion vector in response to said sum values.

2. The circuit according to claim 1, wherein said first circuit comprises a plurality of processing elements each configured to generate one of said difference values.

3. The circuit according to claim 2, wherein said processing elements are logically configured as a two-dimensional array receiving said pixels from said current block and said reference block on a first side of said array and presenting said difference values on a second side of said array.

03-0838
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4. The circuit according to claim 1, wherein said second circuit comprises a plurality of adder circuits each configured to generate one of said sum values substantially simultaneously.

5. The circuit according to claim 4, wherein each of said adder circuits comprises a plurality of stages connected in series, (i) a first of said stages receives a portion of said difference values and (ii) a last of said stages generates said one
5 sum value.

6. The circuit according to claim 1, wherein said third circuit comprises:

an adder circuit configured to generate a plurality of first intermediate values from said sum values;

5 a storage circuit configured to generate a plurality of second intermediate values from said first intermediate values as said current block is moved through a search window; and

a select circuit configured to generate said motion vector from said second intermediate values.

03-0838
1496.00329

7. The circuit according to claim 6, wherein each of said second intermediate values corresponds to one of a plurality of partition modes for said current block for variable block size motion estimation.

8. The circuit according to claim 1, wherein said third circuit is further configured to generate a sum of absolute difference value corresponding to said motion vector.

9. The circuit according to claim 1, wherein each of said sum values corresponds to a smallest partition of said current block.

10. The circuit according to claim 1, wherein (i) said first circuit comprises a plurality of processing elements each configured to generate one of said difference values, (ii) said second circuit comprises a plurality of first adder circuits each configured to generate one of said sum values and (iii) said third circuit comprises:

a second adder circuit configured to generate a plurality of intermediate values from said sum values;

03-0838
1496.00329

10 a storage circuit configured to generate a plurality of
second intermediate values from said intermediate values as said
current block is moved through a search window; and

a select circuit configured to generate said motion
vector from said second intermediate values.

11. A method for motion estimation, comprising the steps
of:

5 (A) generating a plurality of difference values by
calculating an absolute difference between each pixel from a
current block and a corresponding pixel from a reference block
substantially simultaneously;

(B) generating a plurality of sum values by adding said
difference values; and

10 (C) generating at least one motion vector in response to
said sum values.

12. The method according to claim 11, wherein step (C) comprises the sub-step of:

generating a plurality of first intermediate values from
5 said sum values, one of said intermediate values for each of a plurality of partitions of said current block.

13. The method according to claim 12, wherein step (C) further comprises the sub-step of:

generating a plurality of minimum values by retaining a smallest of said sum values for each of said intermediate values as
5 said current block is moved through a search window.

14. The method according to claim 13, wherein step (C) further comprises the sub-step of:

generating a plurality of second intermediate values in response to said minimum values.

15. The method according to claim 14, wherein step (C) further comprises the sub-step of:

generating said motion vector by determining a best of said second intermediate values.

03-0838
1496.00329

16. The method according to claim 11, wherein step (B) comprises the sub-step of:

generating a plurality of first intermediate values by adding a plurality of said difference values.

17. The method according to claim 16, wherein step (B) further comprises the sub-step of:

generating a plurality of second intermediate values by adding a plurality of said first intermediate values.

18. The method according to claim 11, wherein step (A) comprises the sub-step of:

generating a plurality of intermediate values each by calculating a difference between one of said pixels from said
5 current block and one of said pixels from said reference block.

19. The method according to claim 18, wherein step (A) further comprises the sub-step of:

generating said difference values by calculating an absolute difference value for each of said intermediate values.

03-0838
1496.00329

20. A circuit comprising:

means for generating a plurality of difference values by
calculating an absolute difference between each pixel from a
current block and a corresponding pixel from a reference block
5 substantially simultaneously;

means for generating a plurality of sum values by adding
said difference values substantially simultaneously; and

means for generating at least one motion vector in
response to said sum values.